CONDUCTIVE STRUCTURE FABRICATION PROCESS USING NOVEL LAYERED STRUCTURE AND CONDUCTIVE STRUCTURE FABRICATED THEREBY FOR USE IN MULTI-LEVEL METALLIZATION

This application claims the priority of U.S. provisional application no. 60/200,002, filed April 27, 2000, the disclosure of which is expressly incorporated by reference herein.

BACKGROUND OF THE INVENTION

Multi-level metallization is commonly used in the integrated circuit industry to interconnect various components of a circuit and a system. Metals or metal alloys, such as copper or copper alloys, are used in these structures due to their low resistivity. Figures 1(a)-1(c) show an example of the fabrication of two parallel metal lines or other conductive structures in an insulator layer (oxide) 50 grown on a substrate. In this example, copper (Cu) is used as the conductor.

First, a barrier layer 52 and a seed layer 54 are deposited over the whole structure as shown in Figure 1(a). A layer 100 of Cu is then deposited as shown in Figure 1(b), by a technique such as electroplating, over the seed layer. The barrier layer, which remains, is not shown in Figure 1(b). An etching, electrochemical etching, or chemical mechanical polishing (CMP) process is then carried out to remove the copper from the field regions 58 and

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leave it in the channels or other types of features 56 formed in the insulator layer as shown in Figure 1(c).

The process of Figures 1(a)-1(c) depicts an ideal situation. In practice, it is extremely difficult to obtain the structure of Figure 1c. Figure 2 shows the actual cross section of a structure that one may get. Defects, such as dishing 60 and copper remnants 62, can be observed in the channels or other features 56 and over the field regions 58, respectively. Dishing presents a problem because it produces a non-planar surface and increases the resistance of the line. Copper remnants can cause shorts between conductive lines. These defects can be caused by the CMP process (incomplete removal from the field regions and too much removal from the features or channels) as well as by the etching process or the electroetching process.

Figure 3(a) is a view similar to Figure 1(b) but is somewhat enlarged and shows the barrier layer 52, which is not shown in Figure 1(b). Figure 3(a) also shows only one channel or other type of feature 56 and two adjacent field regions 58. Feature or channel dimensions can vary widely, but in order to roughly illustrate the scale of the illustrations provided by Figures 3(a)-3(d), it will be assumed that the feature width W in Figure 3(a) is 100μm and the feature depth D is 6 μm. Figure 3(a) also

illustrates, schematically, the small-grained structure of the Cu layer 100 deposited over the barrier layer 52 on the insulator layer 50.

Conventionally, after the Cu layer 100 has been deposited on the barrier layer overlying the insulator layer 50 as shown in Figure 3(a), the Cu layer is annealed so as to enlarge its grain structure. Figure 3(b) illustrates, schematically, the relatively large-grained structure of the Cu layer 100 after annealing.

The etching, electrochemical etching, or CMP process carried out to remove Cu from the field regions 58 is conventionally performed after the annealing operation. Figure 3(c) shows the structure of the copper layer 100 after the layer has been partially removed from over the field regions 58 by the etching, electroetching, or CMP process. Figure 3(d) shows the insulator layer and barrier layer structure, with a copper conductive structure remaining in the line, i.e. the channel or other type of feature 56, after the copper layer has been completely removed from the field regions 58 by the selected process. Figure 3(d) also shows dishing 60 in the copper conductive structure left in the channel or other feature 56 which results from the conventional copper deposition, annealing and copper removal process.

SUMMARY OF THE INVENTION

The present invention proposes an approach to overcome the dishing and copper (or other conductor) remnant problems mentioned by establishing a structural difference between conductor layers in different regions on the substrate surface. More specifically, the present invention relates to a particular process for fabricating conductive structures in features of an insulator layer on a substrate, to a layered structure used in such a process, and to conductive structures produced by the process. According to the process, a layer of conductive material is applied over the insulator layer so that the layer of conductive material covers field regions adjacent the features and fills in the features. A grain size differential between the conductive material which covers the field regions and the conductive material which fills in the features is then established by annealing the layer of conductive material, and excess conductive material is removed to uncover the field regions and leave the conductive structures.

The layer of conductive material is applied so as to define a first layer thickness over the field regions and a second layer thickness in and over the features. The first layer thickness and the second layer thicknesses are dimensioned such that $d_1 \leq 0.5d_2$, with d_1 being the first layer thickness and d_2 being the second layer thickness. Preferably, the first and second layer

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thicknesses are dimensioned such that $d_1 \leq 0.3d_2$.

According to one embodiment of the invention, the layer of conductive material over the insulator layer is applied by depositing the layer of conductive material over the insulator layer, and partially removing the layer of conductive material from over the field regions to establish a desired thickness differential between the first and second layer thicknesses. According to another embodiment of the invention, the layer of conductive material over the insulator layer is applied by depositing a planarized layer of conductive material over the insulator layer to establish a desired thickness differential between the first and second layer thicknesses.

The layered structure is used in the process and includes the insulator layer on the substrate as well as the layer of conductive material covering the field regions and filling in the features. A grain size differential between the conductive material which covers the field regions and the conductive material which fills in the features is established in the conductive material layer by annealing.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1(a) is a partial cross-sectional view of a patterned

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insulator layer grown on a substrate surface and having overlying barrier and seed layers.

Figure 1(b) is a view similar to Figure 1(a) showing the insulator layer and Cu layer structure after copper deposition but prior to removal of Cu from over the field regions.

Figure 1(c) is a view similar to Figure 1(b) but showing an ideal structure after Cu has been removed from over the field regions.

Figure 2 is an illustration of defects which may occur when a conventional copper deposition, annealing, and copper removal process is carried out.

Figure 3(a) is a somewhat enlarged view similar to Figure 1(b) showing the small grain structure of the Cu layer as deposited.

Figure 3(b) is a view similar to Figure 3(a) but showing the large grain structure of the deposited Cu layer following an annealing operation which conventionally takes place between Cu deposition and removal of Cu from over the field regions.

Figure 3(c) is a view similar to Figure 3(b) but showing the

annealed Cu layer after it has been partially removed from over the field regions.

Figure 3(d) is a view similar to Figure 3(c) showing a dishing defect in the Cu remaining in an insulator layer channel or other feature after Cu has been completely removed from the field regions according to a conventional process.

Figure 4 is a partial cross-sectional view of a layered structure, similar to Figure 1(b), showing a Cu layer according to the invention, after annealing, with large grain structure in certain regions and small grain structure in other regions.

Figure 5 is a cross-sectional view of a planarized, un-annealed Cu film according to a first embodiment of the invention.

Figure 6 is a cross-sectional view similar to Figure 5 but of a partially polished, un-annealed Cu film according to a second embodiment of the invention.

Figures 7(a)-7(c) illustrate sequential operations forming part of an inventive process including use of the Cu film shown in Figure 6.

Figure 8 is a cross-sectional view, similar to Figure 1(c), showing an improved conductive structure, barrier layer, and insulator layer structure, without dishing or conductor remnants, which can be obtained by the invention.

Figure 9 is a cross-sectional view similar to Figure 8 but showing a conductive structure extending beyond adjacent field regions.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 4 represents a novel conductive material layer deposited over a patterned insulator structure. The barrier layer 52 remains disposed between the deposited material, which will be presumed to be Cu, and the insulator layer 50. The novel conductive material layer shown in Figure 4 is distinguished from the conductive material layer shown in Figure 3(b) in that the novel layer includes built in differences in both chemical properties (corrosion rate, etching rate, reactivity, etc.) and structure (grain size, crystal orientation, porosity/density, etc.). More specifically, the chemical properties and structure of the Cu in and over the channels or various other types of features 56 (hereafter referred to generally as "features") are different from the chemical properties and structure of the Cu over the field regions 58. Over the field regions 58, the Cu deposits have small

grains and possibly low density. In and over the features, on the other hand, the Cu deposits are dense and display large grain structures.

When the copper layer of Figure 4 is subjected to an etching, electrochemical etching, or CMP process, it is possible to adjust the process parameters such that the material over the field regions 58 is removed at a rate which is different from the rate at which the material in and over the features 56 is removed. In other words, the differential built in the film in terms of its structure is translated into a differential in the material removal rate. For example, when the film of Figure 4 is subjected to an appropriately selected CMP step, the chemical removal rate of the small grain regions will be higher than that of the large grain regions. Therefore, the material over the field regions 58 should be cleaned up first, decreasing and/or eliminating the Cu remnant defects shown in Figure 2. Similarly, since the removal rate of material over the features 56 will be smaller, dishing should also be minimized. The same arguments can also be made for etching and electroetching processes, since small grain materials can generally be etched faster in a given etchant. The important concept here is to build a structural difference in material deposited over the field regions and in and over the features of the substrate so that this structural difference can be translated into a difference

between the chemical/mechanical removal rates of two types of material.

One way of obtaining the structure of Figure 4 is to initially deposit the Cu film in a planar manner so that its thickness is larger over the features and smaller over the field regions. In this way, upon annealing, a differential in grain size can be obtained.

Figure 5 is a cross-sectional view of a patterned insulator layer 50 on which an un-annealed, planarized, copper conductor layer or film 100 has been deposited. One feature 56 is shown. The barrier layer 52 remains between the planarized copper conductor layer 100 and the insulator layer 50.

The un-annealed, planarized layer 100 shown in Figure 5 may be obtained in the manner disclosed by commonly assigned U.S. Patent application serial no. 09/201,929, titled METHOD AND APPARATUS FOR ELECTRO CHEMICAL MECHANICAL DEPOSITION, filed December 1, 1998, the disclosure of which is incorporated by reference herein. Other commonly assigned U.S. patent applications also exist that relate to depositing a Cu film on a substrate and then planarizing the deposited film. Attention is directed to U.S. applications serial no. 09/283,024, titled METHOD AND APPARATUS FOR FORMING AN

ELECTRICAL CONTACT WITH A SEMICONDUCTOR SUBSTRATE, filed March 30, 1999; serial no. 09/285,621, titled METHOD AND APPARATUS FOR PLATING AND POLISHING A SEMICONDUCTOR SUBSTRATE, filed April 3, 1999; serial no. 09/373,681, titled METHOD AND APPARATUS FOR DEPOSITING AND CONTROLLING THE TEXTURE OF A THIN FILM, filed August 13, 1999; serial no. 09/398,258, titled NOVEL CHIP INTERCONNECT AND PACKAGING DEPOSITION METHODS AND STRUCTURES, filed September 17, 1999; and serial no. 09/483,095, titled SEMICONDUCTOR WORKPIECE PROXIMITY PLATING METHODS AND APPARATUS, filed January 14, 2000.

Other commonly assigned U.S. applications which may be of interest include serial no. 09/466,014, titled A VERTICALLY CONFIGURED CHAMBER USED FOR MULTIPLE PROCESS; serial no. 09/472,523, titled WORK PIECE CARRIER HEAD FOR PLATING AND POLISHING, filed December 27, 1999; serial no. 09/511,278, titled PAD DESIGNS AND STRUCTURES FOR A VERSATILE MATERIALS PROCESSING APPARATUS, filed February 23, 2000; serial no. 09/544,558, titled MODIFIED PLATING SOLUTION FOR PLATING AND PLANARIZATION AND PROCESS UTILIZING SAME, filed April 6, 2000; serial no. 09/568,584, titled ANODE ASSEMBLY FOR PLATING AND PLANARIZING A CONDUCTIVE LAYER, filed May 11, 2000; and serial no. 09/621,969, titled PAD DESIGNS AND STRUCTURES WITH IMPROVED FLUID DISTRIBUTION, filed July 21, 2000.

It has been found that the particularly desired grain structures represented in Figure 4 will result from annealing the Cu film when the thickness of the deposited Cu film over the field regions and the thickness of the film in and over the features have a certain relationship. Specifically, referring now to Figure 5, the desired grain structures will result when the Cu film thickness d_1 over the field regions 58 and the Cu film thickness d_2 in and over the features are dimensioned such that $d_1 \leq 0.5 d_2$. Most preferably, the thicknesses are dimensioned such that $d_1 \leq 0.3 d_2$.

Once an un-annealed, planarized, copper conductor layer or film 100 as shown in Figure 5 has been deposited over the patterned insulator and its barrier layer, the film 100 is then annealed to establish the grain size differential.

Annealing is performed to enlarge the Cu grains in the features 56 so that the grains become as large as possible and voids are eliminated. Annealing parameters (times and temperatures) can be readily determined by one of ordinary skill in the art of metallurgy. A feature depth D of about 6 μm will be presumed by way of example. It will also be assumed that sufficient un-annealed, planarized, copper conductor film 100 has been deposited so that d_1 in Figure 5 is roughly 3 μm and d_2 in Figure 5 is roughly 9 μm. It is to be understood that these

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dimensions are mentioned as examples only and are not intended to limit the invention in any way. Smaller or larger feature depths D and deposition thicknesses d_1 and d_2 can readily be present. Within this framework, numerous annealing processes are acceptable. Certain examples of annealing processes will be mentioned, but the annealing temperatures and annealing times specified are not to be considered limiting.

Assuming again that copper is the conductor deposited on the patterned insulator, annealing can be performed over temperatures ranging, for example, from about 85°C to about 250°C. These temperatures are not to be considered limiting. Air may be used as an ambient atmosphere when annealing is performed in a temperature range of about 85°C-110°C. In this temperature range, annealing can be performed for one hour or more. At higher temperatures, up to about 250°C, annealing will commonly be performed in an inert or reducing atmosphere to avoid oxidation. At temperatures of about 200°C-250°C, annealing can be performed for shorter times of, for example, 1-5 minutes. These times are not to be considered limiting. In the range of temperatures between about 110°C and 200°C, again, annealing will commonly be performed in an inert or reducing atmosphere. As an example, at a temperature of about 150°C, the copper film 100 could be annealed for approximately one-half hour. Annealing times, however, will depend on the copper

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conductor film thickness and can be determined by one of ordinary skill in the art of metallurgy without undue experimentation.

After annealing, with the Cu film thicknesses d_1 and d_2 having the relationship mentioned above, the grain structure represented in Figure 4 results. Excess annealed copper is then removed by etching, electroetching, or CMP from over the features and over the field regions 58 as will be described.

Various well known chemical compositions are used as etchants and electroetchants for different types of metal films. These compositions are well known to those of ordinary skill in the art of metallurgy. As examples of these well known compositions, for copper, solutions of H_2SO_4 (sulphuric acid) and H_2O_2 (hydrogen peroxide) are commonly used as etchants, while, typically, milder acids, such as H_3PO_4 (phosphoric acid), are used as electroetching solutions. Various etching and electroetching compositions and processes are discussed, for example, in <u>Etching Compositions and Processes</u>, M.J. Collie, Noyes Data Corporation, 1982, p. 3.

The annealed Cu grain size over the field regions 58 (typically less than 0.5 μm diameter, average) is substantially smaller than the annealed Cu grain size in and over the features 56 (typically up to and sometimes exceeding 5 μm, average), which is

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a function of the depth of the features. The density of the annealed Cu over the field regions 58, due to voids and other defects, may be in the 97%-100% range, while the corresponding density of the annealed Cu in and over the features 56 is ideally at 100% and, in reality, will be just about 100%. Although this density differential could improve removal properties, it is more important to have present the differential in grain size represented in Figure 4.

Small grain material has a larger concentration of grain boundaries than large grain material. Grain boundaries are "defective" regions as compared to the bulk of the grain, and are where etching or electroetching occurs. Etchants can be formulated to attack grain boundaries, and the rate of chemical attack or chemical etching for small grain material will be higher than that for large grain material. The same can be said for the rate of electroetching, since the same sort of material removal mechanism is present. Thus, in the example discussed above, excess annealed Cu will be removed, by etching or electroetching, from over the field regions 58 before it is removed from over the features 56.

Removal of excess annealed Cu can also be accomplished by CMP. The removal of any material by CMP, however, involves (1) a chemical reaction component, and (2) a mechanical material removal

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component. In a CMP material process, if the mechanical component of the process is doing most of the material removal, then small grain regions of material can actually have a lower removal rate than that of large grain regions. By contrast, if the chemical component of the CMP process is more dominant, then large grain regions of material will have the lower removal rate. Consequently, in the present application of CMP to remove excess Cu from over the channels 56 and the field regions 58, the CMP process will have to be adjusted so that the chemical component is strong and the small grain regions are removed faster than the large grain regions. Such an adjustment may be performed, for example, by using a relatively reactive chemical composition in the CMP process.

Through the use of etching, electroetching, or a properly selected CMP step, as described, on the grain structure represented in Figure 4, the small grain Cu over the field regions 58 can be removed more quickly than the large grain Cu in and over the features 56, and the structure shown in Figure 8, without dishing or copper remnants, can be obtained.

An alternative way to obtain the structure of Figure 8 is to start with an un-annealed conductive material film deposited in a conventional, non-planar manner as shown in Figure 3(a) and then

perform, in order, partial polishing, annealing, and additional polishing operations. This alternative way will be described with reference to Figures 6 and 7(a)-7(c). The conductive material will again be presumed to be Cu.

Figure 6 is a cross sectional view similar to Figure 5. However, as opposed to Figure 5, which shows a planarized, un-annealed film, Figure 6 shows a partially polished, un-annealed Cu film 100. The structure in Figure 6 corresponds to that shown in Figure 7(b).

Figure 7(a) shows a patterned insulator layer 50, a barrier layer 52, and a layer 100 of small grain Cu. As in the known process of Figures 3(a)-3(d), the layer 100 of Cu is deposited, by a technique such as electroplating, over a seed layer originally present on the barrier layer 52, to obtain the structure shown in Figure 7(a). As deposited, d_1 is approximately equal to d_2. At this point, instead of proceeding directly to an annealing step as in the known process represented in Figures 3(a)-3(d), a partial polishing operation is performed to reduce d_1 and thereby modify the dimensional relationship of d_1 and d_2. It is to be understood that, although a "partial polishing" operation has been referred to, any desired material removal process, such as CMP, etching, or electroetching, could be used. Sufficient small grained Cu is

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removed, by way of the partial polishing operation, from over the field regions 58 so that $d_1 \leq 0.5d_2$. Most preferably, the thicknesses are dimensioned such that $d_1 \leq 0.3d_2$.

After a sufficient amount of Cu has been removed from over the field regions to bring the thickness d_1 and d_2 into the desired relationship, the small grained Cu is annealed. Annealing produces a differential in grain size, represented in the layered structure shown in Figure 7(c), such that after annealing, the Cu grains in and over the features 56 are larger than the Cu grains over the field regions 58. In this sense, the grain structure shown in Figure 7(c) is similar to that shown in Figure 4. The small grain Cu over the field regions, therefore, can be removed more quickly than the large grain Cu in and over the features 56, as explained earlier, by an etching, an electroetching, or an appropriate CMP operation. The structure shown in Figure 8, without dishing or copper remnants, can be obtained during this final material removal operation.

If certain parameters, such as etchant strength, are adjusted in the particular material removal process utilized, then other configurations can be obtained. The cross-sectional view of Figure 9, for example, shows a Cu or other type of conductive structure which actually extends beyond adjacent field regions 58.

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Although the invention has been described in connection with the use of depositing Cu, it is similarly applicable to other conductors (metals and conductive metal alloys) which can be electroplated over a semiconductor substrate. The invention is applicable, for example, to depositing Ni, Au, Pt, Ag, Pd, or Rh on such a substrate.

The foregoing disclosure has been set forth merely to illustrate the invention and is not intended to be limiting. Since modifications of the disclosed embodiments incorporating the spirit and substance of the invention may occur to persons skilled in the art, the invention should be construed to include everything within the scope of the appended claims and equivalents thereof.